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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,859	03/08/2004	Jonathon C. Stiff	2059/US/2	2439
60879	7590	05/16/2007		
BROWNSTEIN HYATT FARBER SCHRECK, PC 410 SEVENTEENTH STREET SUITE 2200 DENVER, CO 80202			EXAMINER HERNANDEZ, WILLIAM	
			ART UNIT 2816	PAPER NUMBER
			MAIL DATE 05/16/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/796,859

Applicant(s)

STIFF ET AL.

Examiner

William Hernandez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 4, 10 and 12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-9, 11 and 13-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>20070419</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicant's amendment filed on 4/19/07 has been received and entered in the case. The amendment and arguments presented therein overcome the prior art rejections, and the informality objections, and therefore, these are withdrawn. In view of the current reconsideration, new grounds of rejections are needed as set forth below. The finality of the previous office action is withdrawn.

Claim Objections

1. Claim 18 is objected to because of the following informalities:

Claim 18 needs to depend from claim 17 instead of claim 11 in order to maintain antecedent basis of the phrase, "the protection transistor".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 11, the limitation, "wherein the pull-down transistor has one end coupled with the floating current mirror" is misdescriptive. This is not shown in any of

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Applicant's drawings. One end is shown coupled to ground (vgnd) while the other end is shown coupled to a transistor (M6/M26) not part of the floating current mirror (M4/M24 and M5/M25).

4. Claims 13 and 15-20 are rejected for inheriting the indefiniteness of parent claim 11.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3 and 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwak et al. (USP 7,064,601 B2).

Kwak's Fig. 3 shows a circuit for generating a reference current, comprising:

a positive feedback loop (Q10 and Q11 increase current I) coupled with a floating current mirror (140; the emitters of Q8 and Q9 are not coupled directly to ground); and
a negative feedback loop (120) diverting current from the floating current mirror, wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating

current mirror does not require the additional MOSFET threshold used by a typical current mirror) as called for in claim 1.

As per claims 2, 3 and 5, the recited limitations are clearly shown in Kwak's Fig. 3.

As per claims 6-9, these claims are merely a method to operate the circuit having structure recited in claims 1-3 and 5. Since Kwak teaches the structure, the method to operate such a circuit is inherently disclosed.

7. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Gillingham (USP 5,144,223).

Gillingham's Fig. 5 shows a circuit providing a current reference, comprising:
a floating current mirror (the emitters are not coupled to ground directly) including a first transistor (11) and a second transistor (9);
at least one resistor (5 and 6) defining a voltage node;
a pull-down transistor (20) coupled with the floating current mirror (via transistor 7); and
an output transistor (16);
wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor 11 is coupled to resistor 5 via transistor 8);
wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor 9 is coupled to the gate of output transistor 16 via inverter 15); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (resistors 5 and 6 are coupled in series with transistor 11 with no diverting paths in-between); and

wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating current mirror does not require the additional MOSFET threshold used by a typical current mirror) as called for in claim 14.

8. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Kobatake (USP 6,204,724 B1).

Kobatake's Fig. 8 shows a circuit providing a current reference, comprising:

a floating current mirror (the emitters are not coupled to ground directly) including a first transistor (P2) and a second transistor (P1);

at least one resistor (R1) defining a voltage node;

a pull-down transistor (N25); and

an output transistor (P3);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor P2 is coupled to resistor R1 via transistor N2);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor P1's gate is coupled to the gate of output transistor P3); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (I_2 and I_1 are mirrored currents); and

wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating current mirror does not require the additional MOSFET threshold used by a typical current mirror) as called for in claim 14.

9. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Morishita et al. (USPAP 2004/0027194 A1).

Morishita et al.'s Fig. 11 shows a circuit providing a current reference, comprising:

- a floating current mirror (the emitters are not coupled to ground directly) including a first transistor (21) and a second transistor (22);

- at least one resistor (R1) defining a voltage node;

- a pull-down transistor (24) coupled with the floating current mirror; and

- an output transistor (NTT);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor 21 is coupled to resistor R1 via transistor 23);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor 22 is coupled to the gate of output transistor NTT); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (i_0 and i_1 are mirrored currents); and

wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating

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current mirror does not require the additional MOSFET threshold used by a typical current mirror) as called for in claim 14.

Allowable Subject Matter

10. Claims 11, 13 and 15-20 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH


TUAN T. LAM
PRIMARY EXAMINER